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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,533	06/27/2001	Joun Ho Lee	8733.460.00	3207
30827	7590	07/05/2005	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP			KIELIN, ERIK J	
1900 K STREET, NW			ART UNIT	
WASHINGTON, DC 20006			PAPER NUMBER	

2813

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/891,533

Applicant(s)

LEE, JOUN HO

Examiner

Erik Kielin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-11,13-15,17 and 18 is/are pending in the application.
- 4a) Of the above claim(s) 4-7 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,8-11,13-15,17 and 18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 April 2005 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 3, 8-11, 13-15, 17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claim 1 was amended to recite the limitation "wherein the light transmission restricting layer formed only beneath at least one of the pixel electrodes positioned between the first and second gate lines." Note the underlined portion is the added portion to the claim. The claim is considered indefinite because it is unclear that which the term "only" modifies. As presently written, the term "only" can modify (1) "beneath" or (2) "positioned between the first and second gate lines." There is support for both features in the specification. Accordingly the metes and bounds of the claims are unclear.

For the purposes of patentability, the claims will be interpreted as best understood. As will be shown herein below, the art already applied to reject the claims forms the light transmission restricting layer “only beneath” the pixel electrode, so it would appear that Applicant means for the term “only” to modify “positioned between the first and second gate lines.” If this is so, then the claims should be written so as to require this. Each of independent claims 8 and 13 presents the same problem.

The remaining claims are rejected for depending from the above rejected independent claims 1, 8 and 13.

4. Claim 3 recites the limitation "the semiconductive layer" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim because claim 1 was amended to remove “a semiconductor layer.”

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,747,830 A (**Okita**).

Regarding independent claim 1, **Okita** discloses a liquid crystal display comprising:
a plurality of gate lines **21a, 21b, 21c**, formed along a first direction (Figs. 3, 11B);

a plurality of data lines **22a, 22b, 22c, 22d**, formed along a second direction substantially perpendicular to the first direction and crossing the gate lines (Figs. 3, 11B);

a plurality of pixel electrodes **16** (Figs. 4, 5), **28** (Figs. 3, 11B) each formed in a pixel area defined by the gate lines and the data lines, the pixel electrodes indicating pictures under control of the corresponding gate lines (Figs. 3, 11B); and

a light transmission restricting layer **13, 14** formed only beneath the pixel electrodes **16** positioned between the first and second data lines **22a, 22b, 22c, 22d** (Figs. 4-5). Because the light transmission restricting layer **13, 14** is formed beneath all of the pixel electrodes, it is formed beneath those pixel electrodes formed between the first and second gate lines.

(See also Okita col. 6, lines 1-22; col. 9, lines 10-43.)

Note that Okita states at col. 1, lines 42-46,

“In the image display unit shown in FIG. 11B, **TFT 23**, storage capacitor **20** and pixel electrode **28** are disposed at **each** intersection of the scanning interconnections **21a, 21b and 21c** and the data interconnections **22a, 22b, 22c and 22d**.” (Emphasis added.)

It is held, absent evidence to the contrary that the “hydrogen supply layer **13**” formed of amorphous silicon (a-Si:H) is a light transmission restricting layer by Applicant's admissions in the specification. (See instant specification at p. 7, first paragraph, for example. See MPEP 2112.)

Regarding claim 2, the liquid crystal display as claimed in claim 1, wherein the light transmission restricting layer **13** is a semiconductive layer (col. 6, lines 1-22).

Regarding claim 3, the liquid crystal display as claimed in claim 2, wherein the semiconductive layer **13** is an amorphous silicon layer (col. 6, lines 1-22).

Regarding claim 17, the light transmission restricting layer is formed beneath all of the pixel electrodes and therefore is necessarily formed beneath the pixel electrodes "controlled by a second scanning [e.g. 21b] line among the scanning lines [21a-21c, etcetera]." Note that the control of certain pixel electrodes by a specific scanning line is a method of intended use and does not have patentable weight in product claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 8-12, 18, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of US 6,608,658 B1 (**Tsujimura et al.**).

Regarding independent claims 8 and 13, **Tsujimura** discloses a liquid crystal display (LCD) device, comprising:

a substrate **10** (Fig. 2E);

an insulating layer **14** formed on the substrate **10** (Fig. 2E; col. 3, lines 40-46) --as further limited by instant claim ;

a plurality of switching devices (called "thin film transistor (hereinafter referred to as TFT) array" at col. 1, lines 8-13) over the substrate **10** and therefore necessarily arranged in a plurality of rows and columns (hence the term "array"), each switching device including an active layer **18** formed on the insulating layer **14** --as further limited by instant claim 10;

a plurality of pixel electrodes **23'** over the substrate **10** in a plurality of pixel areas, the plurality of pixel electrodes being connect to a corresponding one of the switching devices, **TFTs**.

a light transmission restricting layer **18**, formed of amorphous silicon simultaneously with the formation of the active layer **18** of each switching device (sentence bridging col. 3, line 63 to col. 67, line 3; Figs. 2C-2E) --as further limited by instant claims 9, 11, and 13-- the layer **18** of amorphous silicon formed only beneath the plurality of pixel electrodes **23'** (Fig. 2E). Because the light transmission restricting layer **18** is formed beneath all of the pixel electrodes, it is formed beneath those pixel electrodes formed between the first and second gate lines (or gate lines G0 and G1).

It is held, absent evidence to the contrary that the amorphous silicon layer **18** of **Tsujimura** is a light transmission restricting layer by Applicant's admissions in the specification. (See instant specification at p. 7, first paragraph, for example. See MPEP 2112.)

Tsujimura does not describe the particulars of the layout of the TFT array.

APA prior art Fig. 2 discloses a liquid crystal display (LCD) device, comprising:

a substrate **31** (prior art Fig. 3);

a plurality of scanning lines (**G0-Gn**) extending along a first direction (prior art Fig. 2);

a plurality of data lines (**D1-Dn**) extending along a second direction substantially perpendicular to the first direction on the substrate and crossing the scanning lines (**G0-Gn**) (prior art Figs. 1, 2);

a plurality of switching devices (specifically thin film transistors, TFTs; p. 3, lines 8-23) on the substrate arranged in a plurality of rows, each switching device connected to one of the

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scanning lines (G0-Gn) for controlling a switching of the switching device --as further limited by instant claim 15-- and one of the data lines (D1-Dn) for applying data to the switching device, wherein switching devices in each row are connected to a same scanning line, and wherein the rows of switching devices are sequentially scanned by the scanning lines (G0 - Gn) (prior art Fig. 2);

a plurality of pixel electrodes **16**, **36** on the substrate **31** (prior art Figs. 1 and 3) in a plurality of pixel areas defined by the scanning lines (G0-Gn) and the data lines (D1-Dn), the pixel electrodes each being connected to a corresponding one of the switching devices (TFTs) (prior art Figs. 1, 2).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the conventional layout of the **APA** as the layout for **Tsujimura** because the details of the array including the scanning lines and data lines are conventional in the art. One of ordinary skill in the art would further recognize that the **Tsujimura** array of TFTs would be controlled by a plurality of scanning lines and data lines the array of TFTs in order to control each pixel and thereby form a LCD, as suggested by **Tsujimura**.

Regarding claim 12, **Tsujimura** discloses the LCD device of claim 8, further comprising an insulating material **14**, between the light transmission restricting layer **18** and the substrate **10**.

Regarding claim 14, the method of claim 13, further comprising forming a second insulating layer **20** on the light transmission restricting layer **18** before forming the pixel electrodes **23'** (Fig. 2E).

Regarding claim 18, the method of claim 13, wherein the light transmission restricting layer is formed beneath the plurality of pixel electrodes **28** that are controlled by a second

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scanning line (G1) among the scanning lines (G0-Gn). Because the light transmission restricting layer is formed in each pixel region, it is necessarily formed beneath the pixel electrodes controlled by G1.

Allowable Subject Matter

9. The following is a statement of reasons for the indication of allowable subject matter: It is believed that the inclusion of the limitation requiring the light transmission restricting layer be formed beneath at least one of the plurality pixel electrodes positioned between the first and second gate lines and **not** forming the light transmission restricting beneath any of the plurality of pixel electrode positioned between any other gate lines (instant claim 1) would be allowable, while also overcoming the rejection under 35 USC 112(2), presented herein above. Similar wording would make independent claims 8 and 13 allowable except that “the first and second gate lines” are equated to the G0 and G1 scanning lines.

Response to Arguments

10. Applicant's arguments filed 21 April 2005 have been fully considered but they are not persuasive.

Applicant argues that each of the applied references fails to teach the newly added limitation that the light transmission restricting layer be formed only beneath at least one of the plurality of pixel electrodes formed between the first and second gate lines. Examiner respectfully disagrees. The light transmission restricting layer is formed only beneath the pixel electrodes in each of the references and therefore reads on this feature.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached from 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin
Primary Examiner
June 30, 2005